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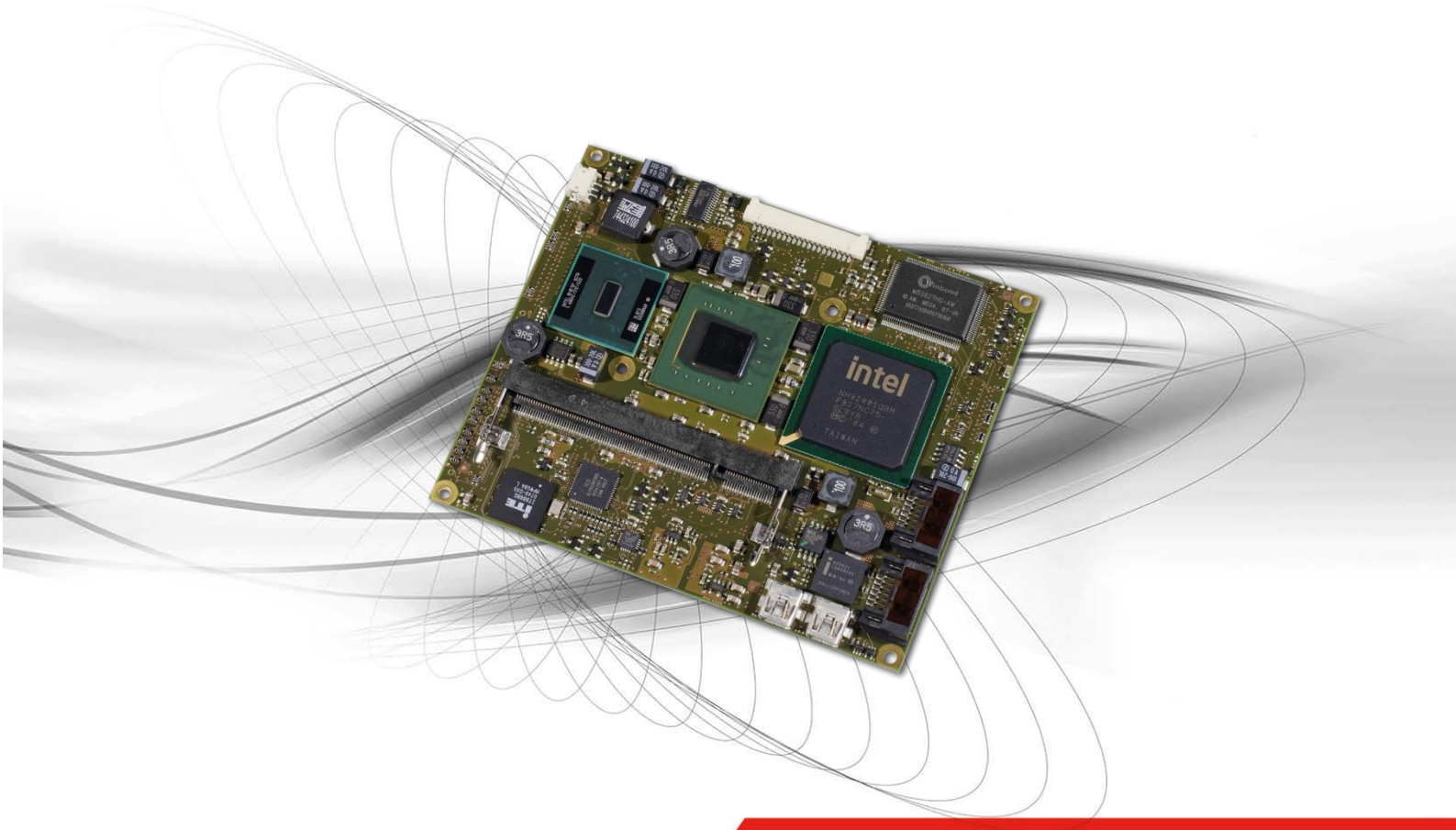

Engineering Leadership

User Manual

ETE/ETX Module
MSC ETE-A945GSE-1

Intel® Atom™ N270

Rev. 0.2

2014-09-19

Preface

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1 General Information

1.1 Revision History

Rev.	Date	Description
0.1	2012-11-28	Draft
0.2	2014-09-19	New covering page

1.2 Introduction

The ETe-A945GSE is an all-in-one Atom™ N270 CPU module. It is fully compliant with the ETX 3.0 standard.

The module is based on Intel® Atom™ N270 CPU and the Intel® 945GSE chipset.

The Intel® Atom™ N270 CPU is on the embedded roadmap of Intel®, which means that the processors are long term available.

The Intel® Atom™ N270 CPU supports 533MHz CPU bus.

The Intel® 945GSE supports 400/533MHz memory bus.

The ETE- A945GSE supports DDR2 memory modules. It provides a 200-pin SO-DIMM socket giving you the flexibility to configure your system up to 2GB of DDR2-DRAM.

The integrated 32-bit 3D Intel® Graphics Media Accelerator 950 supports a dual-channel LVDS graphic interface.

On board features include a 10/100Base-T RTL8103T Ethernet controller, two EIDE ports, audio, parallel / floppy, serial, keyboard and mouse interfaces, six USB2.0 ports and two SATA ports.

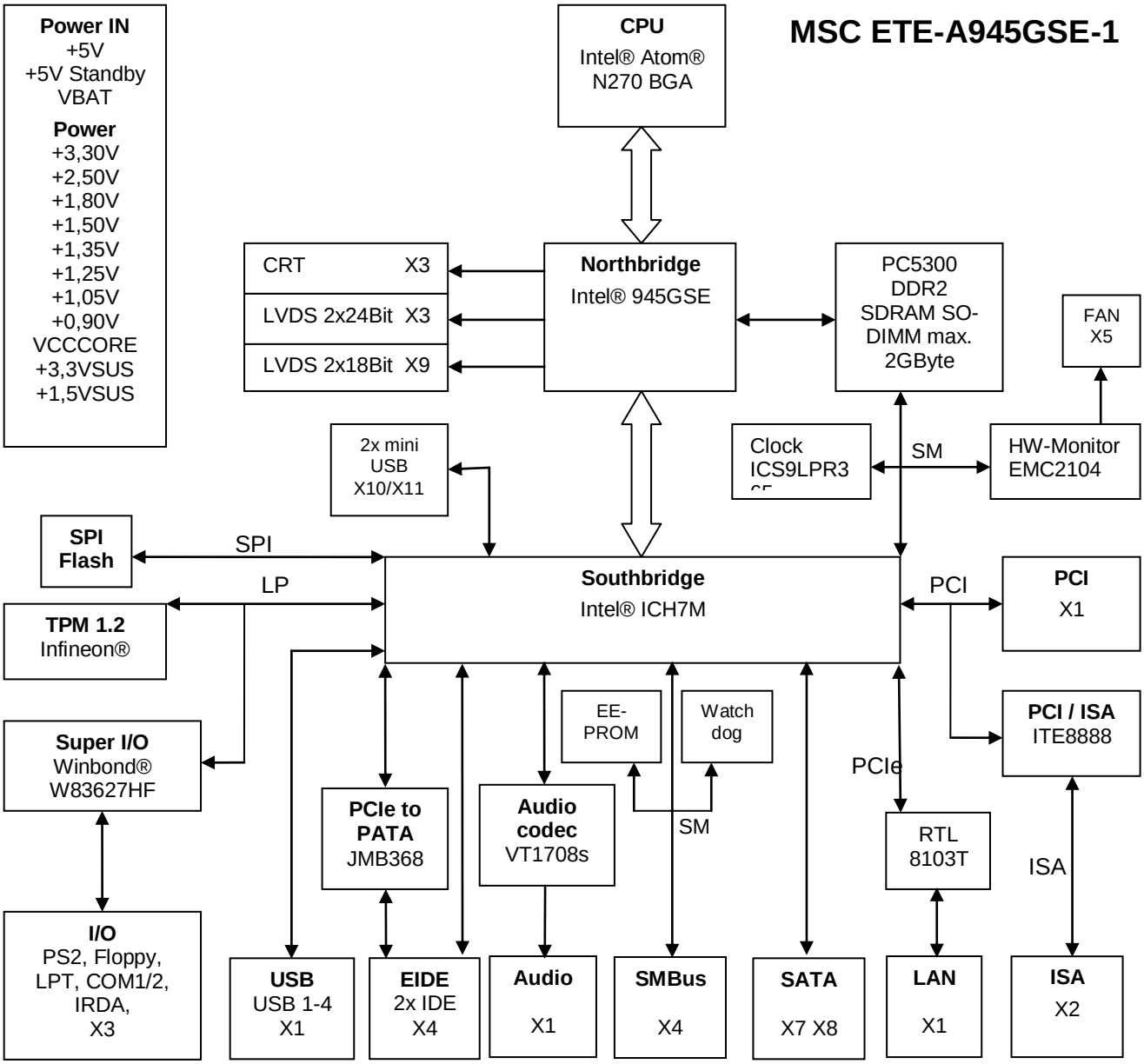
2 Technical Description

2.1 Specifications

Core	
CPU	Intel® Atom ™ Processor N270, 1.60GHz, 533 MHz, FCBGA8, soldered.
ChipSet	Mobile Intel ® 945GSE Intel ® 82801GBM ICH7-M
L2 Cache	512KB 1.60GHz 533 MHz
Memory	200-Pin SO-DIMM socket for DDR2 (max. 2GByte)
ISA-Bus Interface	PCI to ISA Bridge ITE8888 (ETX connector X2)
PCI-Bus Interface	Intel ® 82801 ICH7 (ETX connector X1)
Video	Intel® Gen 3.5 Integrated Graphics Engine CRT-Interface (Optional Flat Panel Interface (LVDS 18bit single-/dual-channel)) Chrontel® CH7308 SDVO to LVDS converter (LVDS 24bit single-/dual-channel)
Ethernet	LAN controller RTL8103T (10/100Base-T)
Audio	HDA decoder VT1708s
USB	integrated in Intel ® 82801GBM ICH7-M: 6 USB 1.1/2.0 ports
EIDE	integrated in Intel ® 82801GBM ICH7-M: 1 Port for up to 2 devices Ultra ATA/66/100 JMICRON® JMB368 PCIe to PATA controller: 1 Port for up to 2 devices Ultra ATA/66/100
Floppy Disk	integrated in W83627 SIO (pins shared with parallel port)
SATA	integrated in Intel ® 82801GBM ICH7-M: 2 Ports
Serial, COM1, COM2	integrated in W83627 SIO: 2 x TTL IrDA on COM2
Parallel	integrated in W83627 SIO: 1 Parallel Port (PS/2-compatible/ECP/EPP via SETUP configurable, pins shared with floppy port)

Keyboard, Mouse	integrated in W83627 SIO: MFII-Keyboard Interface, PS/2-Mouse Interface
Realtime Clock	integrated in 82801GBM ICH7-M (external battery required)
Watchdog	Microcontroller PIC12F509A: Start delay and timeout configurable via SETUP creates hardware reset
TPM (optional)	Trusted Plattform Module TPM 1.2: SLB 9635 TT 1.2
EDID-EEPROM	on Board EDID EEPROM: enable / disable via SETUP
BIOS	Phoenix Trusted/SecureCore in SPI Flash device
EEPROM	EEPROM for CMOS Setup backup
System Monitoring	1 fan with speed input (valid only if optional fan connector is used) 3 temperatures (CPU, GSE and board: EMC2104) 6 voltages (Vcore(CPU), +2.5V, +3.3V, +1.5V, +1.05V, Vbat: W83627 SIO)
Power supply	+5V ±5%
Typical supply current (DOS prompt)	1.6 A
Typical CMOS battery power consumption	1.8 µA RTC / CMOS integrated in Intel ® 82801GBM ICH7-M
Environment	Temperature 0 ... + 60°C (operating), -25 ... + 85°C (non operating) Humidity (rel.) 0 … 95 % (operating), 5 … 95 % (non operating) **Note:** A heat spreader plate is available from MSC providing a standard thermal interface for the module. **The heat spreader is not a heat sink!**
Dimensions	95 x 114 x 12 mm

2.2 Block diagram



2.3 Installation

2.3.1 Jumpers and switches

There are no jumpers or switches.

2.3.2 Installing a DDR2 SO-DIMM module

The ETE-A945GSE board has a standard 200-pin SO-DIMM socket for 1.8V DDR2-SDRAM SO-DIMM modules. The chipset supports 256-Mbit, 512-Mbit and 1-Gbit technologies providing maximum capacity of 2GB.

Note: Module height should not exceed 1260 mil (= 32 mm)

2.4 Watchdog

The ETE- A945GSE board has a watchdog function implemented in a PIC Microcontroller. Via SETUP the watchdog can be enabled and configured.

If the watchdog is enabled a counter is started which creates a reset if it is not retriggered within a programmable time window.

Possible watchdog delays: Disabled (default), 1s, 5s, 10s, 1min, 5min, 10min

The time delay starts before the OS is loaded.

To retrigger the watchdog use the uebi.exe tool.

2.5 Interrupts, DMA channels, Upper memory

IRQ	used for	available	comment
0	Timer 0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2 / COM1	No	(1)
4	COM1 / COM2	No	(1)
5	LPT2 / LPT1	Yes	(1) / (2)
6	Floppy Disk Controller	No	(1)
7	LPT1 / LPT2	No	(1) / (2)
8	Real Time Clock	No	
9	PCI	Yes	(1)
10	PCI / COM3	Yes	(1) / (2)
11	PCI / COM4	Yes	(1) / (2)
12	PS/2 Mouse	No	(1)
13	Floating Point Unit	No	
14	Primary IDE	No	(1)
15	Secondary IDE	No	(1)

(1) If the device is disabled in SETUP, the interrupt is available.

(2) Can be used by external Super I/O controller FDC37C669

2.5.1 PCI Devices

PCI Device	PCI Interrupt	REQ/GNT (0..3)	IDSEL
PCI to ISA ITE8888	serial	4 / 4 5 / 5	AD29
Sound (MODEM, not used)	INTA / INTB	---	
USB 0..3 (Southbridge)	INTC	---	

2.5.2 DMA channels

DMA	used for	available	comment
0		Yes	
1	(ECP, if enabled)	(No)	LPT ECP mode, if enabled
2	Floppy Disk Controller	No	
3	(ECP, if enabled)	(No)	LPT ECP mode (default)
4	Cascade	No	
5..7	- - -	Yes	

2.5.3 Memory map

Upper Memory	used for	available	comment
C0000h..CFFFFh	VGA BIOS	No	64 KB VGA BIOS
D0000h..D3FFFh	SATA	Yes/No	Shared with SATA OPROM*)
D4000h..DFFFFh		Yes	ISA bus or shadow RAM
E0000h..E3FFFh	USB Buffer	No	
E4000h..FFFFFh	System BIOS	No	

*) free when SATA OPROM disabled

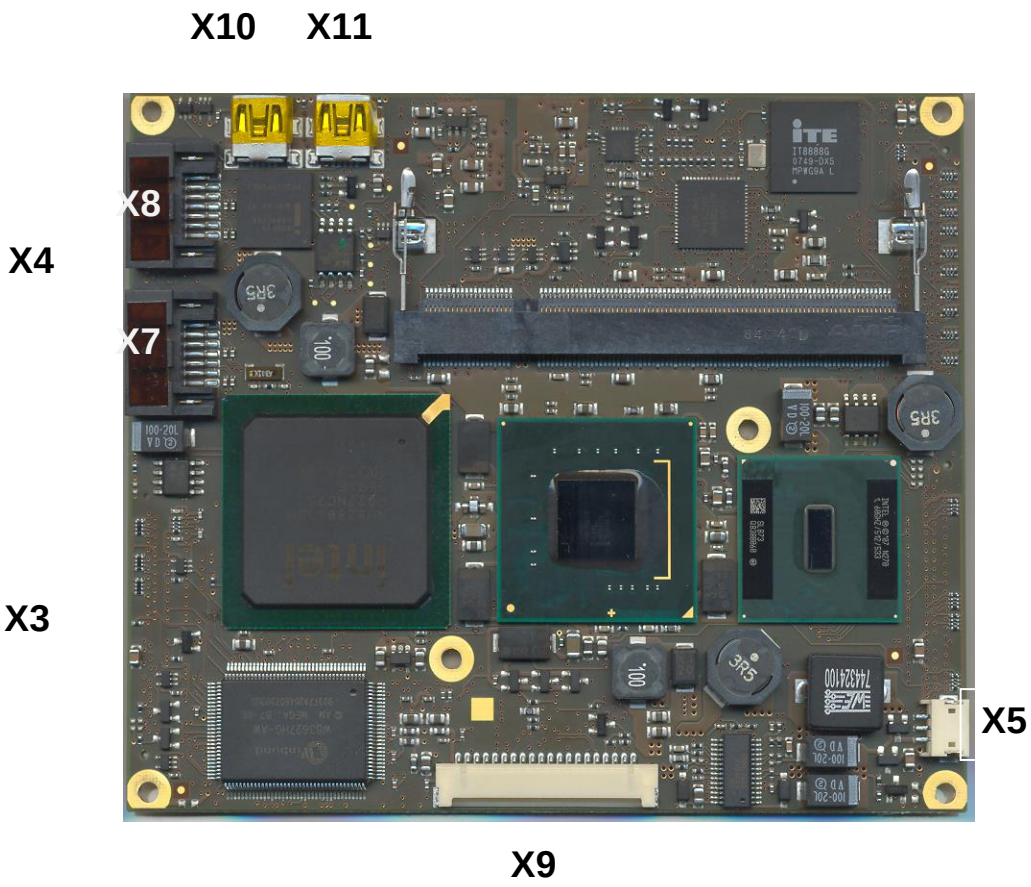
2.5.4 SMBus address map

Device	A6	A5	A4	A3	A2	A1	A0	R/W	address *)
SMBus host	0	0	0	1	0	0	0	x	10_h
clock synthesizer IC9LPRS365	1	1	0	1	0	0	1	x	$D2_h$
watchdog	1	0	1	1	0	0	0	x	$B0_h$
HW monitor EMC2104	0	1	0	1	1	1	1	x	$5E_h$
SIO W83627HF (default)	0	0	1	0	1	1	0	x	$5A_h$
SIO W83627HF Temp3 default	1	0	0	1	0	0	0	x	90_h
SIO W83627HF Temp2 default	1	0	0	1	0	0	1	x	92_h
CMOS backup EEPROM #1	1	0	1	0	1	0	0	x	$A8_h$
CMOS backup EEPROM #2	1	0	1	0	1	0	1	x	AA_h
SPD EEPROM (SO-DIMM)	1	0	1	0	0	0	0	x	$A0_h$

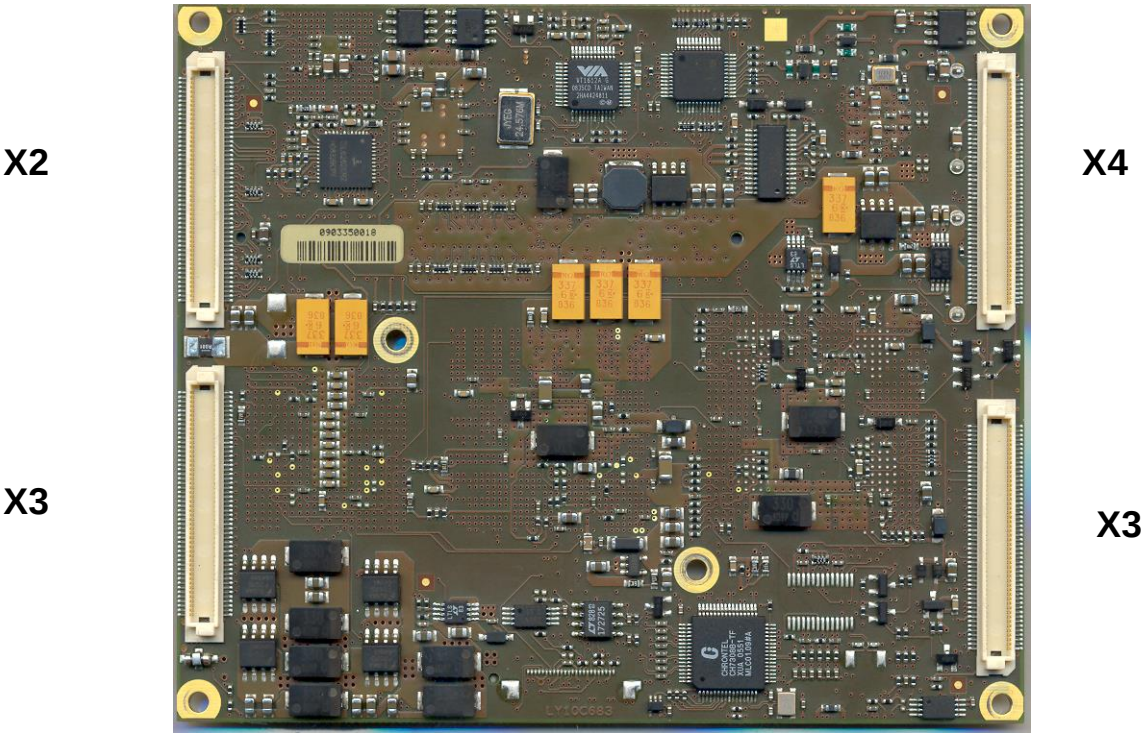
*) 8 bit address (with R/W) / 7 bit address (without R/W)

3 Mechanical Specification

3.1 Top view



3.2 Bottom view



4 ETX Connectors

4.1 Connector X1 (PCI, USB, Audio)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR#
5	GND	6	GND	55	GPERR#	56	RESERVED
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK#	60	DEVSEL#
11	GNT2#	12	3.3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3.3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3.3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

Signal	Description	I/O	Note
VCC	Power Supply +5V, +/-5%	I	external supply
GND	Power Ground	I	external supply
3V	Power Supply +3.3V	O	Do not use externally
RESERVED	Not connected	n.a.	Do not connect

Signal	Description of PCI Bus Signals	I/O	Note
			PCI outputs 3,3V signal level PCI inputs 5V tolerant
PCICLK1..4.	PCI clock output	O	
REQ0..3#	PCI bus request	I	PU 8k2 3,3V
GNT0..3#	PCI bus grant	O	
AD0..31	PCI Adress-/ Databus	I/O	
CBE0..3#	PCI bus command/byte enables	I/O	
PAR	PCI bus parity	I/O	
SERR#	PCI bus system error	I/O	PU 8k2 3,3V
GPERR#	PCI bus grant parity error	I/O	PU 8k2 3,3V
PME#	PCI bus power management event	I/O	internal PU 20k 3,3Vsus
LOCK#	PCI bus lock	I/O	PU 8k2 3,3V
DEVSEL#	PCI bus device select	I/O	PU 8k2 3,3V
TRDY#	PCI bus target ready	I/O	PU 8k2 3,3V
IRDY#	PCI bus initiator ready	I/O	PU 8k2 3,3V
STOP#	PCI bus stop	I/O	PU 8k2 3,3V
FRAME#	PCI bus frame	I/O	PU 8k2 3,3V
PCIRST#	PCI bus reset	O	3,3V signal level
INTA#	PCI bus interrupt A	I	PU 8k2 3,3V
INTB#	PCI bus interrupt B	I	PU 8k2 3,3V
INTC#	PCI bus interrupt C	I	PU 8k2 3,3V
INTD#	PCI bus interrupt D	I	PU 8k2 3,3V
SERIRQ	Serial interrupt request	I/O	PU 10k 3,3V

Signal	Description of USB Signals	I/O	Note
USB0, USB0#	USB Port 0	I/O	5V tolerant; internal PD 15k
USB1, USB1#	USB Port 1	I/O	5V tolerant; internal PD 15k
USB2, USB2#	USB Port 2	I/O	5V tolerant; internal PD 15k
USB3, USB3#	USB Port 3	I/O	5V tolerant; internal PD 15k
USB4, USB4#	USB Port 4	I/O	5V tolerant; internal PD 15k
USB5, USB5#	USB Port 5	I/O	5V tolerant; internal PD 15k

Signal	Description of Audio Signals	I/O	Note
SNDL	Line-Level stereo output left	O	0.7VRMS
SNDR	Line-Level stereo output right	O	0.7VRMS
AUXAL	Auxiliary input A left	I	
AUXAR	Auxiliary input A right	I	
MIC	Microphone input	I	
ASGND	Analog ground of sound controller	I	
ASVCC	Analog supply of sound controller	O	3.3V

4.2 Connector X2 (ISA)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	SD14	4	SD15	53	SA6	54	IRQ5
5	SD13	6	MASTER#	55	SA7	56	IRQ6
7	SD12	8	DREQ7	57	SA8	58	IRQ7
9	SD11	10	DACK7#	59	SA9	60	SYSCLK
11	SD10	12	DREQ6	61	SA10	62	REFSH#
13	SD9	14	DACK6#	63	SA11	64	DREQ1
15	SD8	16	DREQ5	65	SA12	66	DACK1#
17	MEMW#	18	DACK5#	67	GND	68	GND
19	MEMR#	20	DREQ0	69	SA13	70	DREQ3
21	LA17	22	DACK0#	71	SA14	72	DACK3#
23	LA18	24	IRQ14	73	SA15	74	IOR#
25	LA19	26	IRQ15	75	SA16	76	IOW#
27	LA20	28	IRQ12	77	SA18	78	SA17
29	LA21	30	IRQ11	79	SA19	80	SMEMR#
31	LA22	32	IRQ10	81	IOCHRDY	82	AEN
33	LA23	34	IO16#	83	VCC	84	VCC
35	GND	36	GND	85	SD0	86	SMEMW#
37	SBHE#	38	M16#	87	SD2	88	SD1
39	SA0	40	OSC	89	SD3	90	NOWS#
41	SA1	42	BALE	91	DREQ2	92	SD4
43	SA2	44	TC	93	SD5	94	IRQ9
45	SA3	46	DACK2#	95	SD6	96	SD7
47	SA4	48	IRQ3	97	IOCHK#	98	RSTDRV
49	SA5	50	IRQ4	99	GND	100	GND

Signal	Description	I/O	Note
VCC	Power Supply +5V, +/-5%	I	external supply
GND	Power Ground	I	external supply

Signal	ISA Bus Signals	I/O	Note
SD0..15	ISA Databus	I/O	all ISA outputs 5V signal level (PU 8k2 5V) all ISA inputs 5V tolerant
SA0..19	ISA Addressbus	I/O	PU 8k2 5V
LA17..23	ISA Addressbus	I/O	PU 8k2 5V
SBHE#	ISA Byte High Enable	I/O	internal PU 50k 5V
BALE	ISA Address Latch Enable	I/O	PD 4k7
AEN	ISA Address Enable	I/O	PD 4k7
MEMR#	ISA memory read	I/O	PU 8k2 5V
SMEMR#	ISA memory read in lowest 1MB address range	I/O	PU 1k0 5V
MEMW#	ISA memory write	I/O	PU 8k2 5V
SMEMW#	ISA memory write in lowest 1MB address range	I/O	PU 1k0 5V
IOR#	ISA IO read	I/O	PU 8k2 5V
IOW#	ISA IO write	I/O	PU 8k2 5V
IOCHK#	ISA IO check	I	PU 4k7 5V
IOCHRDY	ISA IO channel ready	I/O	PU 1k0 5V
M16#	ISA 16Bit memory device	I/O	PU 1k0 5V
IO16#	ISA 16Bit IO device	I	PU 1k0 5V
REFSH#	ISA memory refresh cycle pending	I/O	PU 1k0 5V
NOWS#	ISA No waitstates	I	PU 1k0 5V
MASTER#	ISA Master	I	PU 1k0 5V
SYSCLK	ISA System clock (8 MHz)	O	
OSC	ISA Oscillator (14,31818 MHz)	O	
RSTDRV	ISA Reset signal	O	
DREQ0..7	ISA DMA request	I	PD 8k2
DACK0#..7#	ISA DMA acknowledge	I/O	
TC	ISA DMA end	I/O	PD 4k7
IRQ3..7	ISA Interrupt request	I	IRQ table see 2.5; PU 8k2 5V
IRQ9..12	ISA Interrupt request	I	IRQ table see 2.5; PU 8k2 5V
IRQ14	ISA Interrupt request	I/O	IRQ table see 2.5; PU 8k2 5V
IRQ15	ISA Interrupt request	I	IRQ table see 2.5; PU 8k2 5V

4.3 Connector X3 (CRT, Display, TVout, Serial, Parallel, Mouse, Keyboard)

Standard pinout with LVDS and LPT

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	LPT/FLPY#	52	RESERVED
3	R	4	B	53	VCC	54	GND
5	HSY	6	G	55	STB#/RES	56	AFD#/DENSEL
7	VSY	8	DDCK	57	RESERVED	58	PD7/RES
9	DETECT#	10	DDDA	59	IRRX	60	ERR#/HDSEL#
11	LCDDO16	12	LCDDO18	61	IRTX	62	PD6/RES
13	LCDDO17	14	LCDDO19	63	RXD2	64	INIT#/DIR#
15	GND	16	GND	65	GND	66	GND
17	LCDDO13	18	LCDDO15	67	RTS2#	68	PD5/RES
19	LCDDO12	20	LCDDO14	69	DTR2#	70	SLIN#/STEP#
21	GND	22	GND	71	DCD2#	72	PD4/ DSKCHG#
23	LCDDO8	24	LCDDO11	73	DSR2#	74	PD3/RDATA#
25	LCDDO9	26	LCDDO10	75	CTS2#	76	PD2/WP#
27	GND	28	GND	77	TXD2	78	PD1/TRK0#
29	LCDDO4	30	LCDDO7	79	RI2#	80	PD0/INDEX#
31	LCDDO5	32	LCDDO6	81	VCC	82	VCC
33	GND	34	GND	83	RXD1	84	ACK/DRV1
35	LCDDO1	36	LCDDO3	85	RTS1#	86	BUSY#/MOT1#
37	LCDDO0	38	LCDDO2	87	DTR1#	88	PE/WDATA#
39	VCC	40	VCC	89	DCD1#	90	SLCT#/ WGATE#
41	JILI_DAT	42	LTGIO0	91	DSR1#	92	MSCLK
43	JILI_CLK	44	BLON#	93	CTS1#	94	MSDAT
45	BIASON	46	DIGON	95	TXD1	96	KBCLK
47	COMP	48	Y	97	RI1#	98	KBDAT
49	SYNC	50	C	99	GND	100	GND

Signal	Description	I/O	Note
VCC	Power Supply +5VDC, 5%	I	external supply
GND	Power Ground	I	external supply
N.C.	Not connected	n.a.	
LTGIO0	General Purpose IO	O	GPIO42; PU 4k7 5V
DETECT#	Not connected	n.a.	

Signal	Description of analog CRT signals	I/O	Note
HSYNC	Horizontal Sync	O	3V3 signal level
VSYNC	Vertical Sync	O	3V3 signal level
R	Red channel RGB Analog Video Output	O	
G	Green channel RGB Analog Video Output	O	
B	Blue channel RGB Analog Video Output	O	
DDCK	Display Data Channel Clock	I/O	PU 2k2 5V
DDDA	Display Data Channel Data	I/O	PU 2k2 5V

Signal	Description of TV signals (option)	I/O	Note
SYNC	n.c.	n.a.	
Y	n.c.	n.a.	
C	n.c.	n.a.	
COMP	n.c.	n.a.	

Signal	Description of COMx signals	I/O	Note
			All TTL signal level
DTR1..2#	Data terminal ready of COM1/COM2	O	
RI1..2#	Ring indicator of COM1/COM2	I	PU 470k 5V
TXD1..2	Data transmit of COM1/COM2	O	
RXD1..2	Data receive of COM1/COM2	I	PU 470k 5V
CTS1..2#	Clear to send of COM1/COM2	I	PU 470k 5V
RTS1..2#	Request to send of COM1/COM2	O	
DCD1..2#	Data carrier detect of COM1/COM2	I	PU 470k 5V
DSR1..2#	Data set ready of COM1/COM2	I	PU 470k 5V

Signal	Description of keyboard and infrared signals	I/O	Note
KBDAT	Keyboard Data	I/O	PU 8k2 5V
KBCLK	Keyboard Clock	O	PU 8k2 5V
MSDAT	Mouse Data	I/O	PU 8k2 5V
MSCLK	Mouse Clock	O	PU 8k2 5V
IRTX	Infrared Transmit	O	
IRRX	Infrared Receive	I	

Signal	Description of FDC signals (shared with LPT)	I/O	Note
LPT/FLPY#	LPT or Floppy Interface configuration input	I	Connect to GND; PU 10k 5V
STB#/RES	nc	-	
AFD#/DENSEL	density select: low = 250/300Kb/s high = 500/1000Kb/s	O	
PD0/INDEX#	Index signal	I	
PD1/TRK0#	Track signal	I	
PD2/WP#	Write protect signal	I	
PD3/RDATA#	Raw data read	I	
PD4/DSKCHG#	Disc changed	I	
PD5/RES	nc	-	
PD6/RES	nc	-	
PD7/RES	nc	-	
ERR#/HDSEL#	Head select	O	
INIT#/DIR#	Direction	O	
SLIN#/STEP#	Motor step	O	
ACK/DRV1	Drive 1 select	O	
BUSY#/MOT1#	Motor 1 select	O	
PE/WDATA#	Raw write data	O	
SLCT#/WGATE#	Write enable	O	

Signal	Description of LPT signals (shared with FDC)	I/O	Note
LPT/FLPY#	LPT or Floppy Interface configuration input	I	Connect to VCC (resistor 4K7); PU 10k 5V
STB#/RES	Strobe signal	O	
AFD#/DENSEL	Automatic feed	O	
PD0/INDEX#	Databus D0	I/O	
PD1/TRK0#	Databus D1	I/O	
PD2/WP#	Databus D2	I/O	
PD3/RDATA#	Databus D3	I/O	
PD4/DSKCHG#	Databus D4	I/O	
PD5/RES	Databus D5	I/O	
PD6/RES	Databus D6	I/O	
PD7/RES	Databus D7	I/O	
ERR#/HDSEL#	LPT error	I	
INIT#/DIR#	Initiate	O	
SLIN#/STEP#	Select	O	
ACK/DRV1	Acknowledge	I	
BUSY#/MOT1#	Busy	I	
PE/WDATA#	Paper empty	I	
SLCT#/ WGATE#	Power ON	I	

Signal	Description of LVDS Flatpanel signals	I/O	Note
BIASON	n.c. (Display contrast voltage ON)	O	
DIGON	Display Power ON	O	3,3V tolerant
BLON#	Display Backlight ON	O	PU 4k7 5V
LCDDO0	LVDS_L0-	O	
LCDDO1	LVDS_L0+	O	
LCDDO2	LVDS_L1-	O	
LCDDO3	LVDS_L1+	O	
LCDDO4	LVDS_L2-	O	
LCDDO5	LVDS_L2+	O	
LCDDO6	LVDS_LCLK-	O	
LCDDO7	LVDS_LCLK+	O	
LCDDO8	LVDS_L3-	O	(*)
LCDDO9	LVDS_L3+	O	(*)
LCDDO10	LVDS_U0-	O	
LCDDO11	LVDS_U 0+	O	
LCDDO12	LVDS_U 1-	O	
LCDDO13	LVDS_U 1+	O	
LCDDO14	LVDS_U 2-	O	
LCDDO15	LVDS_U 2+	O	
LCDDO16	LVDS_U CLK-	O	
LCDDO17	LVDS_U CLK+	O	
LCDDO18	LVDS_U3-	O	(*)
LCDDO19	LVDS_U3+	O	(*)
JILI_DAT	JILI DATA	I/O	PU 4k7 3,3V
JILI_CLK	JILI CLOCK	I/O	PU 4k7 3,3V

(*) n/a

4.4 Connector X3 - alternate pinout

LPT (LPT/FLPY# = high)				Floppy (LPT/FLPY# = low)			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
51	**LPT/FLPY#**	52	RESERVED	51	**LPT/FLPY#**	52	RESERVED
53	VCC	54	GND	53	VCC	54	GND
55	STB#	56	AFD#	55	RESERVED	56	DENSEL
57	RESERVED	58	PD7	57	RESERVED	58	RESERVED
59	IRRX	60	ERR#	59	IRRX	60	HDSEL#
61	IRTX	62	PD6	61	IRTX	62	RESERVED
63	RXD2	64	INT#	63	RXD2	64	DIR#
65	GND	66	GND	65	GND	66	GND
67	RTS2#	68	PD5	67	RTS2#	68	RESERVED
69	DTR2#	70	SLIN#	69	DTR2#	70	STEP#
71	DCD2#	72	PD4	71	DCD2#	72	DSKCHG#
73	DSR2#	74	PD3	73	DSR2#	74	RDATA#
75	CTS2#	76	PD2	75	CTS2#	76	WP#
77	TXD2	78	PD1	77	TXD2	78	TRK0#
79	RI2#	80	PD0	79	RI2#	80	INDEX#
81	VCC	82	VCC	81	VCC	82	VCC
83	RXD1	84	ACK	83	RXD1	84	DRV
85	RTS1#	86	BUSY#	85	RTS1#	86	MOT
87	DTR1#	88	PE	87	DTR1#	88	WDATA#
89	DCD1#	90	SLCT#	89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK	91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT	93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK	95	TXD1	96	KBCLK
97	RI1#	98	KBDAT	97	RI1#	98	KBDAT
99	GND	100	GND	99	GND	100	GND

4.5 Connector X4 (EIDE, Ethernet, Speaker, Batterie, I2C, SMBus, etc.)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW#	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ	54	PIDE_IOW#
5	PS_ON	6	SPEAKER	55	SIDE_D15	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0	58	PIDE_D15
9	KBINH	10	LILED	59	SIDE_D14	60	PIDE_D0
11	RSMRST#	12	ACTLED	61	SIDE_D1	62	PIDE_D14
13	ROMKBCS#	14	SPEEDLED	63	SIDE_D13	64	PIDE_D1
15	EXT_PRG	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2	68	PIDE_D13
19	OVCR#	20	GPCS#	69	SIDE_D12	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11	74	PIDE_D3
25	SIDE_CS3#	26	SMBALRT#	75	SIDE_D4	76	PIDE_D11
27	SIDE_CS1#	28	DASP_S	77	SIDE_D10	78	PIDE_D4
29	SIDE_A2	30	PIDE_CS3#	79	SIDE_D5	80	PIDE_D10
31	SIDE_A0	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9	84	PIDE_D5
35	PDIAG_S	36	PIDE_A2	85	SIDE_D6	86	PIDE_D9
37	SIDE_A1	38	PIDE_A0	87	SIDE_D8	88	PIDE_D6
39	SIDE_INTRQ	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK#	44	PIDE_INTRQ	93	RXD	94	SIDE_D7
45	SIDE_RDY	46	PIDE_AK#	95	TXD#	96	PIDE_D7
47	SIDE_IOR#	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND

Signal	Description	I/O	Note
VCC	Power Supply +5VDC, 5%	I	external supply
GND	Power Ground	I	external supply
N.C.	Not connected	n.a.	

Signal	Description of IDE signals	I/O	Note
PIDE_D0..15	Primary IDE Databus	I/O	D7: Internal PD11k5
PIDE_A0..2	Primary IDE Addressbus	O	
PIDE_CS1#	Primary IDE chip select channel0	O	
PIDE_CS3#	Primary IDE chip select channel1	O	
PIDE_DRQ	Primary IDE dma request	I	Internal PD 11k5
PIDED_AK#	Primary IDE dma acknowledge	O	
PIDE_RDY	Primary IDE ready	I	PU 4k7 3,3V
PIDE_IOR#	Primary IDE IO read	O	
PIDE_IOW#	Primary IDE IO write	O	
PIDE_INTRQ	Primary IDE interrupt request	I	PU 8k2 3,3V
CBLID_P#	Cable ID primary	I	PD 10k
SIDE_D0..15	Secondary IDE Databus	I/O	D7: Internal PD31k6
SIDE_A0..2	Secondary IDE Addressbus	O	
SIDE_CS1#	Secondary IDE chip select channel0	O	
SIDE_CS3#	Secondary IDE chip select channel1	O	
SIDE_DRQ	Secondary IDE dma request	I	PD 4k7
SIDED_AK#	Secondary IDE dma acknowledge	O	
SIDE_RDY	Secondary IDE ready	I	PU 4k7 3,3V
SIDE_IOR#	Secondary IDE IO read	O	
SIDE_IOW#	Secondary IDE IO write	O	
SIDE_INTRQ	Secondary IDE interrupt request	I	PD 8k2
DASP_S	SATA LED#	OC	Function requires ext. PU to 3V3. Do not pull down!
PDIAG_S	Secondary IDE Master/Slave negotiation	I	
HDRST#	HardDrive reset	O	3,3V signal level

Signal	Description of Ethernet signals	I/O	Note
TXD+, TXD-	Ethernet Twisted Pair transmit signal pair	O	
RXD+, RXD-	Ethernet Twisted Pair receive signal pair	I	
ACTLED	Ethernet activity LED	O	3,3V (10mA sink)
LILED	Ethernet link LED	O	3,3V (10mA sink)
SPEEDLED	Ethernet speed LED, ON at 100Mb/s	O	3,3V (10mA sink)

Signal	Description of Misc. signals	I/O	Note
SPEAKER	Speaker output	O	Internal PD 20k ; 3,3V signal level
BATT	Battery supply	I	3,3V (3,6V max.)
PWGIN	Power good input	I	PU 10k 3,3V
I^2CLK	I^2C Bus Clock	I/O	PU 2k2 3,3V
I^2DAT	I^2C Bus Data	I/O	PU 2k2 3,3V
SMBCLK	SM Bus Clock	I/O	PU 6k8 5V
SMBDAT	SM Bus Data	I/O	PU 6k8 5V
SMBALRT#	SM Bus Alert	I	PU 10k 3,3V_SUS
KBINH	Keyboard inhibit	I	PU 10k 5V
5V_SB	Supply of internal suspend circuit	I	
PS_ON	Power Save ON	O	PU 4k7 5V_SB
PWRBTN#	Power Button	I	Internal PU 20k 3,3V_SUS
OVCR#	Over current detect for USB	I	PU 8k2 3,3V_SUS
ROMKBCS#	n.c.	n.a.	
EXT_PRG#	n.c.	n.a.	
GPCS#	n.c.	n.a.	
GPE1#	n.c.	n.a.	
GPE2#	Ring Input	I	PU 10k 3,3V_SUS
BATLOW#	Batterie low	I	PU 220k 3,3V_SUS
EXTSMI#	External SMI	I	PU 10k 3,3V_SUS
RSMRST#	Resume Reset	I	3,3V signal level

4.6 Connector X5 (FAN)

Pin	Signal
1	GND
2	PWM controlled VCC 5V
3	Fan speed

Connector: JST S3B-ZR-SM4A-TF

4.7 SATA Connectors

Pin	Signal X7		Pin	Signal X8
1	GND		1	GND
2	S1_TX+		2	S2_TX+
3	S1_TX-		3	S2_TX-
4	GND		4	GND
5	S1_RX-		5	S2_RX-
6	S1_RX+		6	S2_RX+
7	GND		7	GND

4.8 Mini USB Connectors

Pin	Signal X10		Pin	Signal X11
1	5V		1	5V
2	USB4_Data-		2	USB5_Data -
3	USB4_Data +		3	USB5_Data +
4	USB_ID4		4	USB_ID5
5	GND		5	GND

4.9 LVDS Connector X9 (option)

Pin	Signal
1	LVDS_A0-
2	LVDS_A0+
3	LVDS_A1-
4	LVDS_A1+
5	LVDS_A2-
6	LVDS_A2+
7	LVDS_A_CLK-
8	LVDS_A_CLK+
9	LVDS_B0-
10	LVDS_B0+
11	LVDS_B1-
12	LVDS_B1+
13	LVDS_B2-
14	LVDS_B2+
15	LVDS_B_CLK-
16	LVDS_B_CLK+
17	GND
18	LVDS_VDD_EN (PD 100k, 3,3V tolerant)
19	LVDS_BKLEN# (PU 4k7 5V)
20	LVDS_BKLT_CTRL (PD 100k, 3,3V tolerant)

Connector: Hirose DF14-20P-1.25H

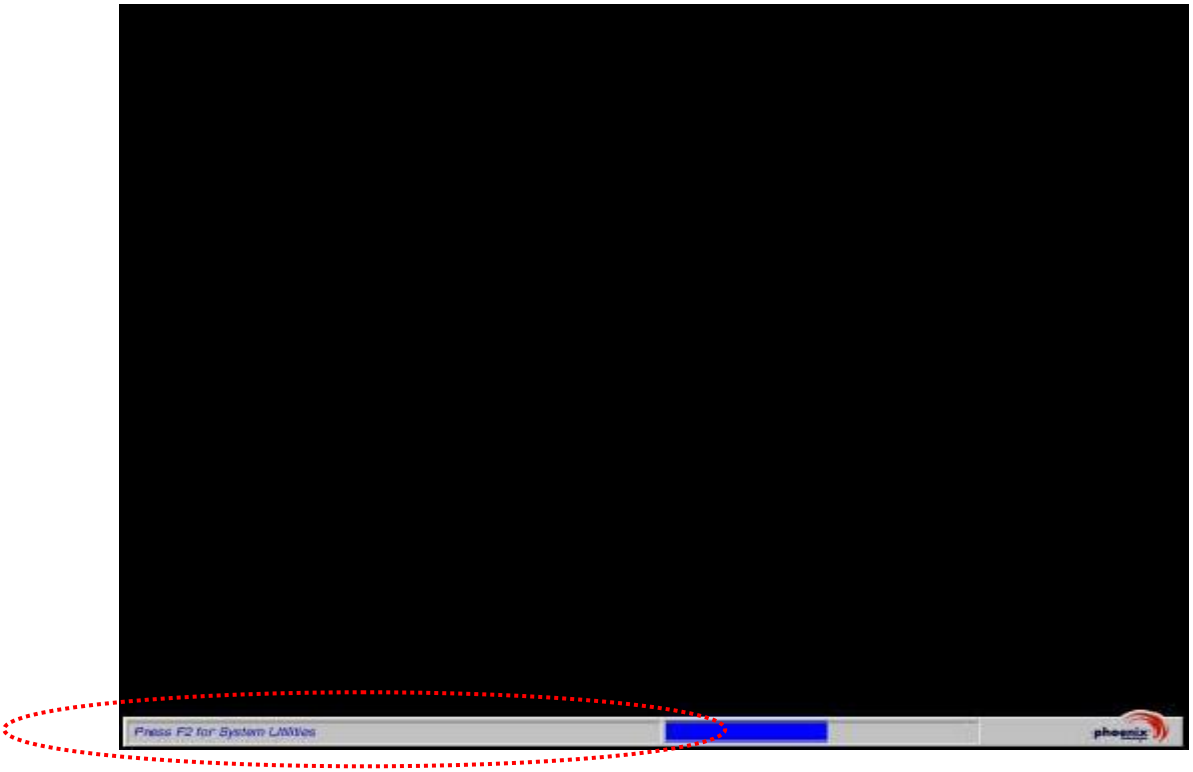
5 BIOS

5.1 Introduction

This guide describes the Phoenix TrustedCore Startup screen and contains information on how to access Phoenix TrustedCore setup to modify the settings which control Phoenix pre-OS (operating system) functions.

5.1.1 Startup Screen Overview

The Phoenix TrustedCore Startup screen is a graphical user interface (GUI) that is included in Phoenix TrustedCore products. The default bios behavior is to show an informational text screen during bios POST phase, but the graphical boot screen can be enabled in the bios setup. The standard boot screen is a black screen, including a progress bar at the bottom of the screen. This bar indicates the progress of the Startup Screen functions and provides user prompting and POST status. The following figure shows the various parts of a generic Startup Screen at 1024x768 resolution:



5.1.2 Activity Detection Background

While the TrustedCore Startup screen is displayed, press the Setup Entry key (F2 – TrustedCore default). The TrustedCore Startup Status Bar acknowledges the input, and at the end of POST, the screen clears and setup launches.

An example of the Startup Status Bar displaying changing state is shown in the following figure. The “Please Wait…” text is displayed after the F2 key is pressed to acknowledge user input.

Active status bar:

5.2 TrustedCore Setup Utility

With the Phoenix TrustedCore Setup program, you can modify TrustedCore settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter provides an overview of the Setup utility and describes at a high-level how to use it.

5.2.1 Configuring the System BIOS

To start the Phoenix TrustedCore Setup utility, press [F2] to launch Setup. The Setup main menu appears.

The BIOS Menu Structure

The BIOS Menu is structured in the following way:

Main	
	Board Information
	IDE Channel 0 Master
	IDE Channel 0 Slave
	SATA Port 0
	SATA Port 1
	Boot Options
Advanced	
	Cache Memory
	CPU Control Sub-Menu
	MCH Control Sub-menu
	Video (Intel IGD) Control Sub-menu
	ICH Control Sub-menu
	PCI Control Sub-menu
	ICH USB Control Sub-menu
	ACPI Control Sub-menu
	Clock Control Sub-menu
	I/O Device Configuration
	Watchdog Options
Security	
Power	
	Hardware Monitor
Boot	
Exit	

The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu Items	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Security	Use this menu to set User and Supervisor Passwords and the Backup and Virus-Check reminders.
Power	Use this menu to configure Power-Management features.
Boot	Use this menu to set the boot order in which the BIOS attempts to boot to OS.
Exit	Exits the current menu.

Use the left and right arrow keys on your keyboard to make a menu selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom of the screen to make your selections, or to exit the current menu. The following table describes the legend keys and their alternates:

Key	Function
F1 or Alt-H	General Help window.
Esc	Exit this menu.
Arrow keys	Select a different menu.
Up and down arrow keys	Move cursor up and down.
Tab or Shift-Tab	Move cursor left and right (i.e. at System Time / System Date).
Home or End	Move cursor to top or bottom of window.
PgUp or PgDn	Move cursor to next or previous page.
F5 or -	Select the previous value for the field.
F6 or + or Space	Select the next value for the field.
F9	Load the Default Configuration values (for all menus).
F10	Save and exit.
Enter	Execute command or select submenu.

Select an item

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

Display a submenu

To display a submenu, use the arrow keys to move the cursor to the sub menu you want. Then press Enter. A pointer marks all submenus.

5.2.2 The Main Menu

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options	Description
Board Information	Submenu	Displays BIOS Version
System Time	Enter Time (HH:MM:SS)	Set the System Time.
System Date	Enter Date (DD/MM/YYYY)	Set the System Date.
IDE Channel 0 Master	Submenu “Master & Slaves”	Configure IDE Channel 0 Master
IDE Channel 0 Slave	Submenu “Master & Slaves”	Configure IDE Channel 0 Slave
SATA Port 0	Submenu “Master & Slaves”	Configure SATA Port 0
SATA Port 1	Submenu “Master & Slaves”	Configure SATA Port 1
Boot Options	Submenu	Configure Boot Options

5.2.2.1 Board Information

Feature	Options	Description
Bios Version	Informative	Shows current bios version.
HW Platform	Informative	Name of the hardware platform
HW Revision	Informative	Hardware revision number
Serial #	Informative	Hardware Serial Number
Boot Counter	Informative	The number of times this board has booted up.
CPU String	Informative	CPU Identification string
CPU Speed	Informative	CPU Speed
CPU Class	Informative	CPU ID Class code
CPU Model	Informative	CPU ID Model code
CPU Stepping	Informative	CPU ID Stepping
CPU Cores	Informative	Number of CPU cores
Northbridge	Informative	Identification of the northbridge
Southbridge	Informative	Identification of the southbridge
System Memory	Informative	Amount of memory below 1MB
Extended Memory	Informative	Total amount of memory

5.2.2.2 Master and Slaves

The **Master** and **Slave** settings on the Main Menu control these types of devices:

- **Hard-disk drives (IDE and SATA)**
- **Removable-disk drives**
- **CD-ROM drives**

There is one IDE connector on your motherboard, usually labeled "Primary IDE". There are usually two connectors on each ribbon cable attached to IDE connector. When you have connected two drives to this connector, the one on the end of the cable is the Master.

When you enter Setup, the Main Menu displays the results of **Autotyping** information each drive provides about its own size and other characteristics–and how they are arranged as Masters or Slaves on your machine.

Note: Do not attempt to change these settings unless you have an installed drive that does not autotype properly (such as an older hard-disk drive that does not support autotyping).

If you need to change your drive settings, select one of the Master or Slave drives on the Main Menu. This will display a menu like this:

Note: The capacity is displayed in 'real' Mbytes (1MB=1024*1024 Bytes) Drives with a total capacity greater than 8Gbyte operate in LBA format only.

Feature	Options	Description
Type	None, ATAPI Removable, CD-ROM, IDE Removable, Other ATAPI, User, Auto	**None** = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. **Auto** = Autotyping, the drive itself supplies the information. **User** = You supply the hard-disk drive information in the following fields. **IDE Removable** = Removable Disk Drive **ATAPI Removable** = Removable Disk Drive **Other ATAPI** = non-specific ATAPI Device **CD-ROM** = CD-ROM drive.
Cylinders	1 to 65536	Number of Cylinders
Heads	1 to 16	Number of read/write heads
Sectors	1 to 63	Number of sectors per track
Multi-Sector Transfers	Disabled, 2 sectors, 4 sectors, 8 sectors, 16 sectors	Any selection except **Disabled** determines the number of sectors transferred per block.

Feature	Options	Description
LBA Mode Control	Disabled, Enabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, & Sectors.
32 Bit I/O	Disabled, Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
Ultra DMA Mode	Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	Ultra DMA Mode supports 33/66/100 MB/sec transfer rate for fixed disk drives.
SMART Monitoring	Disabled, Enabled	Displays the status of SMART Monitoring if supported by the used drive.

WARNING: Incorrect settings can cause your system to malfunction.

5.2.2.3 Boot Options

Feature	Options	Description
Summary screen	Disabled, Enabled	**Enabled** displays system configuration on boot.
Boot-time Diagnostic Screen	Disabled, Enabled	**Enabled** displays the diagnostic screen during boot. **Disabled** displays the Boot Logo.
Post Errors	Disabled, Enabled	Pauses and displays Setup Entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.
Extended Memory Testing	Normal, Just zero it, None	Determines which type of test will be performed on extended memory during POST (above 1 MB).

5.2.3 The Advanced Menu

Feature	Options	Description
Installed O/S	Other, Win95, Win98, WinMe, Win2000, WinXP	Select the operating system installed on your system which you will use most commonly. **NOTE**: An incorrect setting can cause some operating systems to display unexpected behavior.
Reset configuration Data	No, Yes	Select 'Yes' if you want to clear the Extended System Configuration Data (ESCD) area.
Large Disk Access Mode	Other, DOS	Select **Other** for UNIX, Novell NetWare. Select **DOS** for all other operating systems.
Small Disk Access Mode	No, Yes	Select if CHS translation should be made for a LBA-capable harddisk with less than 1024 cylinders, e.g. CompactFlash(R). If you have problems with booting from a CompactFlash(R), try to change this setting. No = translate CHS only if HDD has >1024 cyls. Yes = translate CHS for all LBA-capable disks.
Port 80 Cycles	LPC Bus, PCI Bus	Control where the Port 80h cycles are sent.
Local Bus IDE adapter	Disabled, Enabled	Enable the integrated local bus IDE adapter.
Secondary PATA OPROM	Disabled, Enabled	Enables or disables the OPROM of the onboard secondary PATA Controller
Cache Memory	Submenu	Configure Cache Memory
CPU Control Sub-Menu	Submenu	Configure CPU Control
MCH Control Sub-Menu	Submenu	Configure MCH Control
Video (Intel IGD) Control Sub-Menu	Submenu	Configure Video (Intel IGD) Control
ICH Control Sub-Menu	Submenu	Configure ICH Control
ACPI Control Sub-Menu	Submenu	Configure ACPI Control
Clock Control Sub-Menu	Submenu	Configure Clock Control
I/O Device Configuration	Submenu	Configure I/O Device

Feature	Options	Description
Watchdog Options	Submenu	Configure Watchdog Options

5.2.3.1 Cache Memory Control Menu

Feature	Options	Description
Cache System BIOS area	Uncached, Write Protect	Enables caching of system BIOS area.
Cache Video BIOS area	Uncached, Write Protect	Enables caching of video BIOS area.
Cache D000 – D3FF Cache D400 – D7FF Cache D800 – DBFF	Disabled, Write Through, Write Protect, Write Back	**Disabled** = This block is not cached. **Write through** = Writes are cached and sent to main memory at once. **Write Protect** = Writes are ignored. **Write Back** = Writes are cached but not sent to main memory until necessary.

5.2.3.2 Atom CPU Control Sub-Menu

Feature	Options	Description
Processor Power Management	Disabled, GV3 only, C-States Only, Enabled	Selects the Processor Power Management desired: Disabled = C-States and GV3 are disabled. GV3 Only = C-States are disabled. C-States Only = GV3 is disabled. Enabled = C-States und GV3 are enabled.
Enhanced C-States Enable	Disabled, Enabled	Enables Enhanced C-State support. Disabled = Enhanced C-States disabled. Enabled = Enhanced C-State enable.
Timestamp Counter Updates	Disabled, Enabled	Control TSC updates after C3/C4 through this Setup Option.

Feature	Options	Description
Thermal Control Circuit	Disabled, TM1, TM2, TM1 and TM2	Setting this bit enables the thermal control circuit (TCC) portion of the Thermal Monitor feature of the CPU. TM1 = 50% duty Cycle TM2 = Geyserville III
DTS Enable	Disabled, Enabled	Enabled the Atom DTS to be used for platform Thermal Management. **Note**: If DTS is disabled, thermal throttling in ACPI will not work.
No Execute Mode Mem Protection	Enabled, Disabled	
Set Max Ext CPUID = 3	Disabled, Enabled	Sets Max CPUID extended function value to 3.

5.2.3.3 MCH Control Sub-Menu

Feature	Options	Description
MDA Support	Disabled, Enabled	Control MDA support for the PEG Device.
Memory Throttling	Disabled, Enabled	Controls throttling and bandwidth limiting for the GMCH.
Delta Temperature in SPD	Disabled, Enabled	Controls memory throttling based on thermal information present in the memory SPD.

5.2.3.4 Video (Intel IGD) Control Sub-Menu

Feature	Options	Description
IGD – Device 2	Disabled, Auto	Enables or Disable the Internal Graphics Device by setting item to the desired value.
IGD – Device 2, Function1	Disabled, Auto	Enables or Disable Function 1 of the Internal Graphics Device by setting item to the desired value.
IGD – Boot Type	VBIOS default, CRT, LFP, EFP, EFP2, CRT+LFP, CRT+EFP,	Select the Video Device that will be activated during POST.
IGD – LCD Panel Type	1024x768 1 PPC, 18b 1600x1200 2 PPC, 24b 1280x1024 2 PPC, 24b 1024x768 1 PPC, 24b	Select the LCD panel used by the Internal Graphics Device by selecting the appropriate setup item. The first item is Panel 1, the last item is Panel 16. Some Panels are not numbered due to size constraints. **Note**: Due to size constrains not all Panels are exactly numbered. The first item is Panel 1, the last one Panel 16.
IGD – Panel Scaling	Auto, Force Scaling, Off	Selects the LCD panel scaling option used by the Internal Graphics Device. 1. Auto 2. Force Scaling 3. Off
IGD – Backlight Brightness	0%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100%	Select the starting brightness for the LVDS backlight signal.
DVMT 3.0 Mode	Fixed, DVMT, Combo	Select the configuration of DVMT 3.0 Graphics Memory that Driver will allocate for use by the Internal Graphics Device. 1. Fixed 2. DVMT 3. Combo
Pre-Allocated Memory Size	1 MB, 8 MB	Select the amount of Pre-Allocated Graphics Memory for use by the Internal Graphics Device.
Total graphics Memory	64MB, 128 MB, MaxDVMT	Select the amount of Total Graphics Memory Pre-Allocated + Fixed + DVMT for use by the Internal for use by the Internal Graphics Device.

Feature	Options	Description
DVMT Graphics Memory	N/A	Displays the Memory size of the Video device.
Onboard EDID EEPROM (GSE)	Disabled, Enabled	Enables or disables the Onboard EEPROM for EDID.
Onboard EDID EEPROM (Chrontel)	Disabled, Enabled	Enables or disables the Onboard EEPROM for EDID (Chrontel)

5.2.3.5 ICH Control Sub Menu

Feature	Options	Description
PCI Control Submenu	Submenu	Configure PCI Control
ICH USB Contol Submenu	Submenu	Configure ICH USB Control
AC97A – Device 30, Function 2	Disabled, Auto	Control Detection of the AC97 Audio Device. Disabled = AC97 Audio will be unconditionally disabled, regardless of presence. Auto = AC97 Audio will be enabled if present, disabled otherwise.
AC97M – Device 30, Function 3	Disabled, Auto	Control Detection of the AC97 Modem Device. Disabled = AC97 Modem will be unconditionally disabled, regardless of presence. Auto = AC97 Modem will be enabled if present, disabled otherwise.
AC97 Modem PNE Enable	Disabled, Enabled	Control the ability to wake the System from an AC97 Modem Device
SATA – Device 31, Function 2	Compatible, Enhanced	Compatible: SATA Drive = Primary on SATA Controller, in Legacy Mode. PATA Drive = Secondary on SATA Controller, in Legacy Mode Enhanced: SATA Drive = Primary on SATA Controller, in Native Mode. PATA Drive = Primary on PATA Controller, in Legacy Mode
AHCI Configuration	Disabled, Enabled	Enhanced AHCI: WinXP-SP1+IAA driver supports AHCI mode.

Feature	Options	Description
Disable Vacant Ports	Disabled, Enabled	Controls automatic disabling if vacant SATA ports.
On–board LAN	Disabled, Enabled	Setting item to “Disabled” will remove the LAN from PCI Config Space. Setting item to “Enabled” will allow the LAN to operate correctly.
PXE OPROM	Disabled, Enabled	Enable PXE Option ROM.
Pop Up Mode Enable	Disabled, Enabled	Select the proper mode: If disabled, bus master traffic is a break event and it will return from C3/C4 to C0 based on break events. If enabled, ICH will observe a bus master request and it will take the system from a C3/C4 state to a C2 state and auto enable bus masters.
Pop Down Mode Enable	Disabled, Enabled	Should be enabled only if Pop up is enabled: If disabled, ICH will NOT attempt to automatically return. If enabled, ICH will observe a NO bus master request and it can return to a previous C3 or C4 state.
DMI Link ASPM Support	Enabled, Disabled	Control ASPM support for DMI link between GMCH and ICH.

5.2.3.5.1 PCI Control Sub-Menu

Feature	Options	Description
PCI IRQ line 1 - 8	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 12	Select the IRQ number that should be used for this PCI interrupt line. Disabled – PCI INT not functional Auto Select – Let Bios decide which IRQ should be assigned 3, 4, 5, 6, 7, 10, 12 – Use this IRQ number for the PCI interrupt **Note:** To avoid a critical conflict with SMBUS it is not possible to disable IRQ line 4.

5.2.3.5.2 ICH USB Control Sub-Menu

Feature	Options	Description
USB 1.1 Controllers	Enable 1, Enable 2, Enable 3, Enable 4	Select the number of enabled USB1.1 Controllers.
USB 2.0 Controller	Disabled, Enabled	Control USB 2.0 functionality through this Setup Item.

5.2.3.6 ACPI Control Sub-Menu

Feature	Options	Description
Enable ACPI	No, Yes	En/Disable ACPI BIOS (Advanced Configuration and Power Interface)
Disable ACPI _Sx	None, S1, S2, S3	Select one of the ACPI power states: S1, S2, or S3. If selected, the corresponding power state will be disabled.
FACP – RTC S4 Flag Value	Disabled, Enabled	Valid only for ACPI Control the value for the RTC S4 flag in the FACP Table
FACP – PM Timer Flag Value	Disabled, Enabled	Valid only for ACPI Controls the timer used by the OS through the FACP Tables Flags. This is now possible with WINXP SP2 and beyond.
HPET Support	Disabled, Enabled	This field is valid only in the WindowsXP OS. Control the High Performance Event Timer through this setup option when enabled. The HPET Table will then be pointed to by the RSDT and the proper enable bits will be set.
HPET Base Address	0xFED00000, 0xFED01000, 0xFED02000, 0xFED03000	Select the Base Address for the High Performance Event Timer.
Passive Cooling Trip Point	Disabled, 47 C, 55 C, 63 C, 71 C, 79 C, 87 C, 95 C, 103 C, 111 C, 119 C	This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the CPU. Note: If the DTS is enabled, only values below 97C are valid.

Feature	Options	Description
Passive TC1 Value, Passive TC2 Value,	0 - 15	This value sets the TC1-2 value for the ACPI Passive Cooling Formula.
Passive TSP Value	1 - 15	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled.
Critical Trip Point	POR, 47 C, 55 C, 63 C, 71 C, 79 C, 87 C, 95 C, 103 C, 111 C, 119 C, 127 C	This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off. Notes: (1)100C is POR for all Intels CPUs. (2) If value is > 100C and DTS is enabled, the Out-of-Spec Bit will be used. (3) The EC value will be set to 127 after ACPI initialation.

5.2.3.7 Clock Control Sub-Menu

Feature	Options	Description
CK-505 Clock Chip	Program	Control Programming of the CK-505 Clock Chip. Program = TBD.
PLL1 Spread Spectrum Mode	Off, Down Spread, Center Spread	Programming of PLL1 Spread Spectrum Clock Off : PLL1 Spektrum is disabled Down Spread = 0.5% Center Spread = 0.25%
PLL3 Spread Spectrum	Off, Software	Programming of PLL3 Spread Spectrum Clock Off : PLL1 Spektrum is disabled Software = Spread Spectrum is Bios Controlled with following supported ranges : Down Spread: 0.5% - 2% Center Spread: 0.25% - 0.5%
Spread Percentage	Down 0.5%, Down 1%, Down 1.5%, Center 0.25%, Center 0.5%	If controlled by Software, select Percentage of PLL3 Spread Spectrum

5.2.3.8 I/O Device Configuration Menu

Feature	Options	Description
Serial Port A	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port A.
Interrupt	3, 4	Set the interrupt for Serial Port A.
Serial Port B	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Mode	Normal, IR, ASK-IR	Set the mode for Serial Port B (wired / infrared).
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port B.
Interrupt	3, 4	Set the interrupt for Serial Port B.
Parallel Port	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Mode	Output only, Bi-directional, ECP	Set the mode for Parallel Port.
Base I/O address	378, 278, 3BC	Set the base I/O address for Parallel Port.
Interrupt	5, 7	Set the interrupt for Parallel Port.
DMA channel	1, 3	Set the DMA channel for Parallel Port (only available if mode was set to ECP).

Warning: If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting settings.

5.2.3.9 Watchdog Options

Feature	Options	Description
Watchdog delay	1 second, 5 seconds, 10 seconds, 30 seconds 1 minute, 5 minutes, 10 minutes, 30 minutes	After watchdog is activated, he waits selected delay time before he starts counting the timeout period.
Watchdog timeout	0.4 second, 1 second, 5 seconds, 10 seconds, 30 seconds, 1 minute, 5 minutes, 10 minutes	Select the maximum watchdog trigger period. If the watchdog will not be triggered during selected period, system reset will be generated.
Watchdog start on boot	No, Yes	Select if the watchdog should be started at the end of POST.

5.2.4 The Security Menu

Feature	Options	Description
Supervisor Password Is	Displays Supervisor Password Is	Displays the current status of the Supervisor password (“Clear” or “Set”)
User Password Is	Displays User Password Is	Displays the current status of the User password (“Clear” or “Set”)
Set Supervisor Password	Press return to enter supervisor password	Supervisor Password controls access to the setup utility.
Set User Password	Press return to enter user password	User Password controls access to the system at boot.
Password on boot	Disabled, Enabled	Enables password entry on boot
TPM Support	Disabled, Enabled	Enable Trusted Platform Module support.
Current TPM State	Displays Current TPM State	Displays the current TPM status.
Change TPM State	No Change, Enable & Activate, Deactivate & Disable, Clear	Changes TPM state.

5.2.5 The Power Menu

Feature	Options	Description
After Power Failure	Stay Off, Power On	Sets the mode of operation if an AC power loss occurs. Power On will turn the power on as soon as the power supply is back on. Stay Off will keep the power off until the power button is pressed.
Hardware Monitor	Submenu	Configure Hardware Monitor

5.2.5.1 Hardware Monitoring Menu

Feature	Description
CPU Vcore	Displays the current CPU voltage.
Supply voltage (+5V)	Displays the current voltage.
CPU Temperature Sensor	Displays the current CPU temperature.
Board Temperature Sensor	Displays the current board temperature.
FAN 1 speed	Displays the current fan speed.

5.2.6 The Boot Menu

After you turn on your computer, it will attempt to load the operating system (such as DOS, Windows XP or Linux) from a device listed in the boot priority order. If it cannot find the operating system on that device, it will attempt to load it from the next device in that list.

Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD ROMs, removable devices (e.g. USB sticks), and network cards.

Note: Specifying any device as a boot device on the Boot Menu requires the availability of an operating system on that device.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

Feature	Description
Boot priority order: 1: USB KEY: 2: USB FDC: 3: IDE 4: 4: IDE 5: 5: IDE 0: 6: IDE 2: 7: PCI LAN: 8:	Boot priority order for next boot. System tries to boot the first bootable device in this list. Use <+> and <-> to change order. Use <x> to exclude or include device to boot priority list.
Exclude from boot order: : IDE 1: : IDE 3: : USB HDD: : USB CDROM: : USB ZIP: : USB LS120: : PCI SCSI:	System does not try to boot a device from this list.

Pressing the “F10” key during the bios boot phase will bring up the bios boot menu, which will allow you to select a different boot device for the current boot process only. In this boot menu, only devices in the “Boot priority list” will selectable. Devices excluded from boot order will not be shown.

5.2.7 The Exit Menu

The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Exit Saving Changes

After making your selections on the Setup menus, always select "Exit Saving Changes". This procedures stores the selections displayed in the menus in CMOS (short for "battery-backed CMOS RAM") a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.

If you attempt to exit without saving, the program asks if you want to save before exiting. During boot-up, PhoenixBIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu.

If, during boot-up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

System CMOS checksum bad - run SETUP Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press <F1> to resume the boot or <F2> to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

Selecting “Discard Changes” on the Exit menu updates all the selections with their previous values.

Save Changes

Selecting “Save Changes” saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

5.3 Bios Update

If a System-BIOS update is required please follow these instructions:

1.) Create a bootable DOS disk/usb-stick/hdd.
2.) Copy PHLASH16.EXE, BIOS.WPH and UPDATE.BAT to this device.
3.) Boot the system from this device.
4.) Type "update.bat" to update the System BIOS.
5.) When the BIOS update has finished, reboot the system.

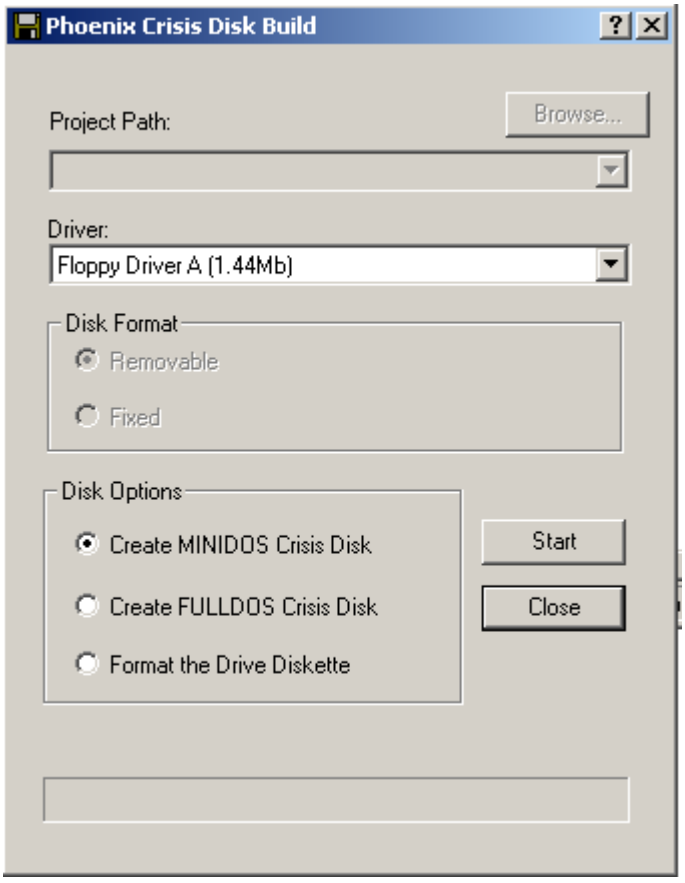
Note: After the system has been updated, the CMOS has been changed to defaults and therefore it is necessary to enter Setup (press F2 at boot time) to configure the system settings.

5.4 Bios Crisis Recovery

Note: Contact your sales for information how to get the CRISDISK.ZIP and an USB recovery dongle.

Please follow these simple steps to create a bootable crisis recovery medium:

Unzip CRISDISK.ZIP and start the windows-based program WINCRIS.EXE on the host system. A window will pop up as shown below:



In the drop-down box, either select “Floppy Drive A” to create a recovery disk, or select “Removable Disk 0 (xxxMb)” to create a recovery usb stick. Disk options should be left at “Create MINIDOS Crisis Disk”.

Press the start button to generate the selected crisis recovery medium.

There are two possibilities to force the target system into crisis recovery mode: either by USB crisis recovery dongle or by crisis recovery jumper.

With the dongle, you just have to plug it into a free USB port before switching the system on. Please make sure that you use different USB controllers for USB dongle and USB crisis recovery medium. After powerup, crisis recovery mode should automatically start.

The crisis recovery jumper is located next to Com Express Board Connector the (see picture below). You have to shorten the two pins before applying power to the board. As soon as crisis recovery is started, you can remove the jumper.

The programming process is signalled by short beeps and terminated after successfull programming with one long beep. After that, the system is automatically rebooted.

Important Notes:

USB recovery dongle and USB crisis recovery device must not be plugged to the same USB controller.

Crisis recovery may take up to 5 minutes

A long beep indicated successful recovery

Crisis recovery does not include the bootblock.

5.5 Diagnostics Postcodes

Postcodes can be seen on a special Postcode display, either on the MSC mainboard or on an external Postcode PCI card. There is an item in the bios setup to select the bus that should get the postcode data: either PCI (for external cards) or LPC (for onboard displays).

If a postcode display has only 2 digits, only the lower byte of word-value postcodes will be shown.

5.5.1 Bootblock Bios Postcodes

Code	Bootblock Task Description
BBH	Bootblock Early Init after Reset
80h	Chipset Init
81h	Bridge Init
82h	CPU Init
83h	System Timer Init
84h	System I/O Init
85h	Check forced Recovery Boot, CMOS & CMOS Backup Clear
86h	Check BIOS Checksum
87h	Goto BIOS, start early BIOS initialzations
88h	Init Multi Processor
89h	Set Huge Segment
8Ah	OEM Initializations
8Bh	Init Interrupt and DMA Controller
8Ch	Init Memory Type
8Dh	Init Memory Size
8Eh	Shadow Boot Block
8Fh	Init SMM
90h	System Memory Test
91h	Init Interrupt Vectors
92h	Init Realtime Clock
93h	Init Standard Video
94h	Init Beeper
95h	Initialize USB Controller
95h	Init Boot
96h	Clear Huge Segment
97h	Boot OS
99h	Init Security

5.5.2 System Bios Postcodes

Code	Beeps	POST Task Description
04h		Get CPU type
03h		Disable Non-Maskable Interrupt (NMI)
06h		Initialize system hardware
07h		Disable shadow and execute code from the ROM.
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component
0Fh		Initialize fixed disk drives
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1-2-2-3	BIOS ROM checksum
17h		Initialize cache before memory Autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable Interrupt Controller
20h	1-3-1-1	Test DRAM refresh
22h	1-3-1-3	Test 8742 Keyboard Controller
24h		Set ES segment register to 4 GB
28h		Autosize DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 kB Base RAM
2Ch	1-3-4-1	RAM Address test
2Eh	1-3-4-3	Base RAM Test
2Fh		Enable cache before system BIOS shadow
32h		Compute CPU clock speed in MHz
33h		Initialize Phoenix Dispatch Manager
36h		Warm start shut down
38h		Shadow system BIOS ROM
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
41h		Initialize RomPilot
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2-1-2-3	Check ROM copyright notice
47h		Initialize I20 support

Code	Beeps	POST Task Description
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
4Fh		Initialize MultiBoot
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled
55h		Configure USB devices
58h	2-2-3-1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press F2 to enter SETUP"
5Bh		Disable CPU cache
5Ch		Conventional memory test
60h		Extended memory test
62h		Address Test on Extended Memory
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		CPU feature, MP, and APIC initialization
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display BIOS shadow status
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Dh		Initialilze Intelligent System Monitoring
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialisation
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports.
87h		Configure Motheboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area

Code	Beeps	POST Task Description
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Program timing registers according to PIO modes
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1-2	Enable PCI devices and ROM Scan One long, two short beeps on checksum failure
99h		Check for SMART Drive
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives
A0h		Set time of day
A2h		Check key lock
A4h		Initialize typematic rate
A8h		Erase F2 prompt
AAh		Scan for F2 key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B1h		Inform RomPilot about the end of POST.
B2h		POST done - prepare to boot operating system
B3h		store enhanced CMOS values in non-volatile area
B4h		1 One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)
B7h		Initialize ACPI BIOS
B9h		Prepare Boot
BAh		Initialize DMI parameters
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Check virus and backup reminders
C0h		Try to boot with INT 19
C1h		Initialize POST PEM Error Manager
C2h		Initialize PEM error logging
C3h		Initialize error PEM display function
C4h		Initialize PEM system error handler

Code	Beeps	POST Task Description
C5h		PnPnd dual CMOS (optional)
C6h		Initialize note dock (optional)
C7h		Initialize note dock late
C8h		Force check (optional)
C9h		Extended checksum (optional)
CAh		Redirect Int 15h to enable remote keyboard
CBh		Redirect Int 13h to Memory Technologies
CCh		Redirect Int 10h to enable remote serial video
CDh		Remap I/O and memory for PCMCIA
CEh		Initialize digitizer and display message
D2h		Unknown interrupt or exception

5.5.3 Memory Detection Postcodes

Code	Calistoga Memory Detection
FFA0h	Start memory detection
FF01h	Enable MCHBAR
FF02h	Check for DRAM initialisation interrupt and reset fail
FF03h	Verify all DIMMs are DDR2 and unbuffered
FF04h	Detect an improper warm reset and handle
FF05h	Detect if ECC SO-DIMMs are present in the system
FF06h	Verify all DIMMs are single or double sided and not asymmetric
FF07h	Verify all DIMMs are x8 or x16 width
FF08h	Find a common CAS latency between the DIMMS and the MCH
FF09h	Determine the memory frequency and CAS latency to program
FF10h	Determine the smallest common TRAS for all DIMMs
FF11h	Determine the smallest common TRP for all DIMMs
FF12h	Determine the smallest common TRCD for all DIMMs
FF13h	Determine the smallest refresh period for all DIMMs
FF14h	Verify burst length of 8 is supported by all DIMMs
FF15h	Determine the smallest tWR supported by all DIMMs
FF16h	Determine DIMM size parameters
FF17h	Program Graphics frequency and PLL settings
FF18h	Program system memory frequency
FF19h	Determine and set the mode of operation for the memory channels
FF20h	Program clock crossing registers
FF21h	Disable Fast Dispatch
FF22h	Program the DRAM Row Attributes and DRAM Row Boundary registers
FF23h	Program the DRAM Bank Architecture register
FF24h	Program the DRAM Timing & and DRAM Control registers
FF25h	Program ODT
FF26h	Perform steps required before memory init
FF27h	Program the receive enable reference timing control register Program the DLL Timing Control Registers , RCOMP settings
FF28h	Enable DRAM Channel I/O Buffers
FF29h	Enable all clocks on populated rows
FF30h	Perform JEDEC memory initialization for all memory rows
FF31h	Program PM Settings
FF32h	Perform additional steps required after memory init
FF33h	Program DRAM throttling and throttling event registers
FF34h	Setup DRAM control register for normal operation and enable
FF35h	Setup DRAM control register for normal operation and enable
FF36h	Enable RCOMP
FF37h	Clear DRAM initialization bit in the ICH

5.5.4 ACPI Postcodes

Code	ACPI Codes
03h	Enter Suspend State S3
04h	Enter Hibernate State S4
05h	Enter Softoff State S5
ABh	Enter Wakeup from Powerstate
CDh	End Wakeup from Powerstate

6 Troubleshooting

For additional help contact MSC Technical Support:
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